III. REMARKS

Claims 1-18 are pending in this application. The following remarks are being made to facilitate early allowance of the presently claimed subject matter. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the following remarks is respectfully requested.

In the Office Action, claims 1, 2, 8-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kanehira et al. (USPN 6,212,671 B1); claims 3 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kanehira et al. in view of Chang et al. (USPN 6,370,579); and claims 4, 5, 7 and 13-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kanehira et al. in view of Woodbright (USPN 5,640,497). Applicants respectfully traverse these rejection and request withdrawal for the reasons stated below.

1. Kanehira et al., Woolbright, or Chang et al., either separately or in the suggested combination, do not disclose or suggest each and every claimed feature of the current invention.

Kanehira et al. disclose an apparatus and a method for automatically producing a mask pattern. *See* e.g., col. 11, lines 60-66. The Kanehira et al. method includes a "region specifying step" (ST1), a "cell layout specifying step" (ST2), a "wiring line layout specifying step" (ST3), an "isolation region pattern producing step" (ST4), and a "layout verifying step" (ST5). *See* col. 12, line 15 – col. 13, line 44. Basically, the Kanehira et al. method produces certain mask patterns and verifies "whether the contents of the mask patterns produced in the proceeding steps meet the wafer processing information 1 and the logic information 2[.]" Col. 13, lines 40-43. Applicants submit that Kanehira et al. does not disclose or suggest, *inter alia*, the following features of the current invention.

a) Kanehira et al., do not disclose or suggest, *inter alia*, "restating the instruction algorithm in terms of at least two fundamental algorithms[,]" as recited in claim 1 and claimed similarly in claims 10 and 13 of the current invention. In the current invention, as disclosed in the specification, "[a] 'fundamental algorithm' is an instruction that represents a convenient restating or grouping of element(s) used in an instruction algorithm and, hence, convenient restating or grouping of design layer(s)." Paragraph 24 of the current application. In Kanehira et al., the mask patterns are created based on wafer processing information, logic information, cell information and core information. *See* col. 12, line15 - col. 13, line 40. Kanehira et al. do not disclose or suggest any "fundamental algorithm," and it is apparent that the information of Kanehira et al. are not "fundamental algorithms" because the information is not even an instruction.

The Office asserts that "the first and the second logic circuit forming regions" of Kanehira et al. are fundamental algorithms. Office Action at page 2. Applicants respectfully traverse this assertion, because the first and second logic circuit forming regions are all objects of the mask pattern producing method (apparatus), and are not instructions.

b) Kanehira et al., do not disclose or suggest, *inter alia*, "creating a graphical representation for each fundamental algorithm[,]" as recited in claim 1 and claimed similarly in claims 10 and 13 of the current invention. In Kanehira et al., wafer processing information, logic information, cell information and core information are used in ST1-ST5 for the determination of the mask pattern, however, these four kinds of information are used together. For example, in step ST1, all four kinds of information are used. *See* col. 12, lines 20-25. In step ST3, both logic information and cell information are used. Col. 12, lines 53-55 ("on the basis of the logic information 2 ... and cell information 3"). Kanehira et al. do not disclose or suggest creating a graphic representation for ***each*** of the wafer processing information, logic information, cell information and core information.

The Office asserts that Kanehira et al. disclose creating a graphical representation for each fundamental algorithm by disclosing that "a graphic data processing operation is carried out to increase the sizes of the first logic circuit forming region[.]" Office Action at page 2 (internal citation omitted). Applicants respectfully traverse this assertion. In the Office Action, the Office already asserts that the first logic region is a "fundamental algorithm." Office Action at page 2. Following the Office's logic, to increase the sizes of the first logic circuit forming region is to increase the size of a "fundamental algorithm," which is not creating a physical representation for the "fundamental algorithm." The more fundamental deficiency of the Office's assertion is that Kanehira et al. do not include a fundamental algorithm, as the above analysis shows.

c) Kanehira et al. do not disclose or suggest, *inter alia*, "combining the graphical representations corresponding to each fundamental algorithm according to the restated instruction algorithm to form a combined graphical representation[,]" as recited in claim 1 and claimed similarly in claims 10 and 13 of the current invention. In Kanehira et al., the mask pattern layout data are determined step by step (e.g., ST1-ST5) based on the four kinds of information (wafer processing information, logic information, cell information and core information). In each step, the four kinds of information are used together and there is no graphical representation created for each fundamental algorithm, as the above analysis explains. Consequently, Kanehira et al. do not disclose or suggest combining the graphical representations corresponding to each fundamental algorithm.

In the Office Action, the Office asserts that Kanehira et al. include the combining feature because in Kanehira et al., "the graphic information is added for correction to the information about the well walls 108b and 208b[.]" Office Action at page 2. Applicants respectfully traverse this assertion. In Kanehira et al., the graphic information is obtained by comparing the calculated results (regarding, e.g., spaces between the well wall 108b and the N-type wells 104) and the predetermined values. *See* col. 15, lines 38-47. That is, in Kanehira et al., the graphic information is not a graphical

representation corresponding to each fundamental algorithm. Consequently, the addition of the graphic information to the information about the well walls 108b and 208b is not "combining the graphical representations corresponding to each fundamental algorithm[.]"

d) Kanehira et al. do not disclose or suggest, *inter alia*, "electronic comparison between the combined graphical representation and a graphical representation based on the article[,]" as recited in claim 1 and claimed similarly in claims 10 and 13 of the current invention. In Kanehira et al., step ST5 verifies "whether the contents of the mask patterns produced in the proceeding steps meet the wafer processing information 1 and the logic information 2[.]" Col. 13, lines 40-43. That is, Kanehira et al. compare mask pattern layout data with the data (information) that is used to create the mask pattern layout data. By sharp contrast, in the current invention, the comparison is between combined graphical representations (for each fundamental algorithm) and graphical representation based on a (real) article. In Kanehira et al., no graphical representation based on a real article (real mask pattern layout) is involved in the comparison.

In the Office Action, the Office asserts that Kanehira et al. include this comparing feature. After careful review, Applicants respectfully submit that the citations relied by the Office do not support the Office's assertion. For example, the Office cites the Kanehira et al. statement: "the graphical information is added for correction to the information about the well walls 108b and 208b produced in well wall mask pattern to obtain a mask pattern[.]" Office Action at page 3 (inner citation omitted). However, the above citation only shows that Kanehira et al. include correction of information, and it does not disclose or suggest the electronic comparison feature of the current invention.

In addition, the Office cites col. 19, line 13 through col. 21, line 17 of Kanehira et al. to support the assertion that Kanehira et al. include the electronic comparison feature of the current invention. Applicants have reviewed the cited section and found that it is not related to electronic comparison. Applicants respectfully request clarification regarding this citation.

Moreover, the Office asserts that "Kanehira teaches the final mask pattern layout (layer article) data for forming the bottom walls 108 and 208 is determined on the basis of information about increased region" and that " this feature is related to combined graphical representation by adding graphical information for correction." Office Action at page 3. Applicants respectfully submit that the citation only shows that Kanehira et al. is different to the current invention, because the determination is based on "information about increased region," instead of electronic comparison.

Woolbright and Chang et al. do not overcome, *inter alia*, the above identified deficiencies of Kanehira et al.

In view of the foregoing, Applicants respectfully request withdrawal of the rejections

2. Woolbright and Chang et al. are not analogous art.

The claimed invention pertains to, *inter alia*, the creation of a graphical representation for each fundamental algorithm and the verification of a layered article data preparation based on the combined graphical representation, and aims to provide an improved verification. Applicants submit that Woolbright and Chang et al. are not related to a verification of layered article data preparations.

Woolbright relates to "redesigning layouts [by] adjust[ing] polygon data to develop a new layout which meets new design rules." Abstract. In Woolbright, "original data is developed from the layout to be redesigned," and "[t]he original data is then used to create new data," and the original data and created data are broken down into segments, and the broken down data is "then hit with a wave box 26 until the design is optimum 28." Col. 3, lines 41-56. As best understood, Woolbright's system

relates to the revision of an original data representation, i.e., PG data including polygon representations of the actual physical layout, to achieve an optimum redesign of the layout. The current invention does not relate to redesigning a layout, rather it is related to verifying whether a data preparation for a layered article is correct based on a combined graphical representation. In the current invention, a physical chip layout (layered article) never exists and all of the operations are in the stages prior to the actual creation of a physical layout. In contrast, in Woolbright, the redesigning is based on an already existing physical chip layout. In addition, Woolbright is not related to creating a graphical representation for each fundamental algorithm, i.e., instructions on how to generate a layered article, and verification of the layered article data preparations based on the combined graphical representation. In Woolbright, the original data and created data are based on the already existing physical layout instead of a fundamental algorithm that instructs on how to generate a physical layered article. Accordingly, Applicants submit that it is illogic that a person having ordinary skill in the art would consider Woolbright in pursuing verification of a data preparation for articles constructed of multiple design layers.

In addition, Chang et al. is related to "the correction of integrated circuit layouts for optical proximity effects which maintains the original true hierarchy of the original layout." Abstract. Correction of layout design is quite different than verifying design layers that generate the layout. For instance, correction of design layout in Chang et al. and verifying design layers that generate the layout in the current invention are at different stages of designing a layout. Accordingly, Applicants submit that it is illogic that a person having ordinary skill in the art would consider Chang et al. in pursuing verification of a data preparation for articles constructed of multiple design layers.

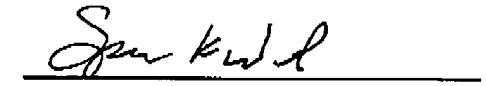
In view of the foregoing, Woolbright and Chang et al. are neither in the same field of the Applicants' endeavor, nor reasonably pertinent to the particular problem with which the Applicants are concerned with this application.

Accordingly, Applicants respectfully request withdrawal of the rejections based on Woolbright or Chang et al.

Claims 2-9 are dependent upon claim 1, claims 11 and 12 are dependent upon claim 10, and claims 14-18 are dependent upon claim 13. The dependent claims are believed to be allowable based on the above arguments, as well as for their own additional features.

Applicants respectfully submit that the application is in condition for allowance. Should the Examiner believe that anything further is necessary to place the application in better condition for allowance, he is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,



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Date: February 17, 2005

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